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jc904 U.S. PTO

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08-14-2000

PATENT APPLICATION

Attorney Docket No. : 00 P 7812 US

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Date of Deposit: August 10, 2000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL LETTER FOR NEW APPLICATION

Sir:

Transmitted herewith for filing is a(n) ☒ Original patent application.
☒ Utility ☐ Design ☐ Continuation-in-part application

INVENTOR(S): Daniel Wu

TITLE: APPARATUS AND METHOD FOR DATA BUFFERING

Enclosed with this transmittal (submitted in duplicate) are the following:

- ☒ 13 page specification.
☒ 4 sheets of drawings ☐ formal drawings ☒ informal drawings (one set)
☒ The Declaration and Power of Attorney ☒ signed ☐ unsigned
☒ An Assignment Transmittal and Assignment to SIEMENS INFORMATION AND COMMUNICATION NETWORKS, INC.
☒ Filing fee has been calculated as shown below (other than small entity):


For	Number Filed	Number Extra	Rate	Additional Fees
Total Claims	16 - 20	= 0	x \$ 18	\$ 0.00
Indep. Claims	5 - 3	= 2	x \$ 78	\$156.00
<input type="checkbox"/> First Presentation of a Multiple Dependent Claim			x \$260	\$ 0.00
			Basic filing Fee	\$690.00
			Total	\$846.00

Please charge my Deposit Account No. 19-2179 in the amount of \$846.00. The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment to Deposit Account No. 19-2179 pursuant to 37 CFR 1.25. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,



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JC675 U.S. PTO
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Smoking status (smoker/non-smoker)	100/100
Alcohol consumption (g/day)	100.0 ± 50.0
Physical activity (hours/week)	10.0 ± 5.0
Comorbidities (hypertension/diabetes/cholesterol)	100/100/100
Medication (antihypertensive/antidiabetic/anticholesterol)	100/100/100
Quality of life (SF-36 score)	100.0 ± 10.0
Health status (good/fair/poor)	100/100/100
Life expectancy (years)	10.0 ± 5.0
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[illegible]

The present invention relates to data storage in data processing devices. More particularly, the present invention relates to methods and apparatus useful in data storage to detect and isolate data corruption due to buffer overwrites.

There is a large body of previous work regarding buffer and memory management and techniques useful for insuring memory integrity and detecting errors.

One situation in which memory corruption can occur is out-of-bounds memory overwrite. In many programming or operating system environments, it can be difficult to ensure that all machine-executed memory writes only write to memory allocated to the particular process or subroutine doing the writing. Consider a case where a physical memory is divided up into n separate buffers, B1 through B n . Oftentimes, some or all of these buffers may be stored essentially contiguously (though not necessarily in order), one after the other, in the memory space.

In some logic system environments, it is difficult to ensure that every memory write to a buffer neither exceeds the buffer size nor falls outside a particular address range. In these systems, a write to buffer B5 may cross the buffer boundary and overwrite data in an adjacent buffer (such as B3). Oftentimes, this erroneous overwrite may not be detected until a subsequent attempt to access data in the overwritten buffer. At that point, it is difficult to determine which process caused the erroneous overwrite and even the attempt to do so may involve a possibly unsuccessful complex recreation of the error condition in a lab, followed by debugging.

The present invention may be understood in the context of a buffer or memory segment system in a memory storage (such as a RAM) or recording device (such as a disk

In a specific embodiment, the first portions and final portions of buffers according to the invention normally will be identical unless an overwrite error has occurred. This will lead to simpler design. However, it will be understood to practitioners in the art from the teachings herein that what is important is that a compare of the first and last portions should indicate if an overwrite has occurred. Thus data may be encoded or formatted somewhat differently in each portion, as long as the essential data is present or can be derived to perform a compare and/or a repair.

While the invention has particular applications in the field of legacy real-time embedded software systems, using the teachings provided herein, it will be understood by those of skill in the art, that the methods and/or apparatus according to the present invention can be advantageously used in other data storage situations. It also will be understood from the teachings herein that the invention can be adapted to many different memory systems and buffer structures, including structures where segments are, for example, not absolutely contiguous.

The invention will be better understood with reference to the following drawings and detailed descriptions. In different figures, similarly numbered items are intended to represent similar functions within the scope of the teachings provided herein. In some of the drawings and detailed descriptions below, the present invention is described in terms of the important independent embodiment of a multimedia message system. This should not necessarily be taken to limit the invention, which, using the teachings provided herein, can be applied to other data accessing situations.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simple block diagram showing a logical buffer organization according to specific embodiments of the invention.

FIG. 2 is a flowchart illustrating a general method for detecting memory errors according to embodiments of the invention.

FIG. 3 is a flowchart illustrating a general method for correction of header errors according to embodiments of the invention.

FIG. 4 is a flowchart illustrating a general method for correction of header errors according to embodiments of the invention.

FIG. 5 is a simple block diagram showing a process space including buffer logic according to specific embodiments of the invention.

FIG. 6 is a diagram illustrating an example computer device that can embody aspects of the present invention.

DESCRIPTION OF SPECIFIC EMBODIMENTS

To aid understanding by the reader, the invention will be explained in the context of various specific memory system configurations as examples. FIG. 1 is a simple block diagram showing a logical buffer organization according to specific embodiments of the invention. As shown in FIG. 1, a buffer system according to specific embodiments of the

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As will be understood in the art, a common overwrite error may occur when data is being written into a buffer such as 110, and the address logic performing the writing indicates an address beyond the boundary of the data portion. In some prior art system, such an overwrite would quickly corrupt data in a different buffer. However, according to the current invention, an overwrite will first overwrite the redundant header, which can then be detected as discussed herein.

A method for repairing a damaged memory segment according to further aspects of the invention is shown in FIG. 3. This method may be understood as beginning upon determining a redundant header is different from an initial header (Step B1). At that point, one of the headers is validated, such as by checking whether a pointer is within a valid range, checking a CRC or checksum, etc. (Step B2). If validated, the validated portion may be copied over the other corrupted portion (Step B3).

An alternative method for repairing a damaged memory segment according to further aspects of the invention is shown in FIG. 4. This method may be used when the top part of a header has been invalidated by an overwrite in a different buffer. The method may be understood as beginning upon determining a redundant header is different from an initial header (Step C1). At that point, the bottom part of the buffer is validated, such as by checking whether a pointer is within a valid range, checking a CRC or

checksum, etc. (Step C2). If validated, the validated bottom part may be copied over the corrupted top part of the buffer (Step C3).

It will be understood to practitioners in the art and from the teaching provided herein that the steps of this method as herein described may be performed in various system configurations and in orders somewhat different from what is specifically illustrated. It will be further understood to practitioners in the art and from the teaching provided herein that the steps of this method, in various embodiments, may be performed in different orders.

A buffer manager according to the invention may be implemented at various logic levels in a software environment. For example, aspects of the invention can be implemented in low level buffer allocation logic (which may be a system resource, usually implemented in a low-level programming language such as C or assembly). In a such a manager, a system according to the invention will be particularly effective in detecting overruns quickly and repairing them and therefore increasing the MTBF. The invention may also be implemented in application level software (in a variety of programming languages). When implemented in an addressing system, a system according to the invention will be particularly effective in isolating the "culprit" that causes an overwrite to occur. To be able to both quickly repair overruns and to detect culprits, aspects of the present invention may be implemented in both a memory manager and in address logic software.

The present invention has thus far been described in terms of general methods and devices. The previous description is believed to be a full and complete description sufficient to allow an ordinary practitioner in the art to make and use the invention. It will be understood to those of skill in the art from the teachings provided herein that the described invention can be implemented in a wide variety of specific data processing system environments and logical systems (such as UNIX, Windows, Solaris, Oracle, etc.) using a wide variety of programming languages (such as SQL, Visual Basic, Pascal, C, C++, Basic, Java, etc.) and wide variety of file formats.

What follows are descriptions of example systems and methods that embody various aspects of the present invention. This following discussion is included, in part, in order to disclose particularly preferred modes presently contemplated for practicing the invention. It is intended, however, that the previous discussion and the claims not be limited by examples provided herein. It is further intended that the attached claims be read broadly in light of the teachings provided herein. Where specific examples are

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described in detail, no inference should necessarily be drawn to exclude other examples known in the art or to exclude examples described or mentioned briefly from the broad description of the invention or the language of the claims. It is therefore intended that the invention not be limited except as provided in the attached claims and equivalents thereof.

Software System Example

Logic according to the present invention may be included either in operating system logic or application logic. As known in the art, this logic may be part executable code that is either stored as software, firmware, or part of the hardware logic of an information device.

In an information processing system according to the invention, the invention may be embodied as modified buffer allocation and write logic, and example of which is illustrated below. For example, buffer write logic according to the invention can be understood by the following pseudo code examples.

Example Logic Flow Buffer Writes

According to the present invention, writes to buffers may be validated as described in the example below. As will be understood to practitioners in the art from the teachings provided herein, in legacy system, it is a common practice to: first allocate a buffer from a system pool; fill in the buffer with some data (in these examples, the data is from some database); and possibly do some massaging of the data at the same time. This may be a very high priority task. After this task is complete, the buffer is then sent to another process for more detail processing. This could be a low priority task. After the processing is done, the process that did the detail processing will release the buffer back into the pool.

Example Prior Art Legacy System Write

```

Buffer_Pointer1 = Allocate_Memory
Index_Pointer1  = Buffer_Pointer1
DBentry_Pointer1 = Points to beginning of database entry 1

Loop
  Content of Index_Pointer1 = Content of DBentry_Pointer1
  Index_Pointer1 incremented to next memory location
  DBentry_Pointer1 incremented to next memory location
  Break out of loop if content of DBentry_Pointer1 is Null
endloop

Send Buffer_Pointer1 to another process

```

Example Buffer Write According to the Invention

```

Buffer_Pointer1 = Allocate_Memory()           //Pointer is returned by
                                              system function that

```

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A system according to the invention may also perform a similar verify when a buffer is requested or returned. How a system is implemented will depend on how much real-time overhead processing a system designer wishes to add for buffer validation. An advantage to validation on buffer allocation is that the validation can potentially repair an

Processor Space Illustration

General Computer Embodiment

FIG. 6 shows an information appliance (or digital device) 700 that may be understood as a logical apparatus that can read instructions from media 717 and/or network port 719. Apparatus 700 can thereafter use those instructions to direct server or client logic, as understood in the art, to embody aspects of the invention. One type of logical apparatus that may embody the invention is a computer system as illustrated in 700, containing CPU 707, optional input devices 709 and 711, disk drives 715 and optional monitor 705. Fixed media 717 may be used to program such a system and may represent a disk-type optical or magnetic media, magnetic tape, solid state memory, etc.. The invention may be embodied in whole or in part as software recorded on this fixed

The invention also may be embodied in whole or in part within the circuitry of an application specific integrated circuit (ASIC) or a programmable logic device (PLD). In such a case, the invention may be embodied in a computer understandable descriptor language which may be used to create an ASIC or PLD that operates as herein described.

The invention has now been described with reference to specific embodiments. Other embodiments will be apparent to those of skill in the art. It is understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested by the teachings herein to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the claims. All publications, patents, and patent applications cited herein are hereby incorporated by reference in their entirety for all purposes.

The invention has now been described with reference to specific embodiments.

1. A method for detecting memory corruption comprising:
performing a data write to a predefined memory segment;
after said write, comparing a redundant portion at the end of said segment to an initial header portion of said segment;
if said comparing indicates that data has been written into said redundant portion,
signaling an overwrite error.
2. A method according to claim 1 wherein said signaling occurs in real-time and can detect and isolate a process causing said erroneous overwrite.
3. A method according to claim 1 wherein said initial portion includes a memory segment header and includes a pointer to a next segment in a linked list.
4. A method according to claim 1 wherein said memory segment is a buffer in a buffer system comprised of a plurality of buffers.
5. A method according to claim 1 further comprising:
if said comparing indicates a difference between said initial portion and said redundant portion, validating one of said portions and copying a validated portion to the location of a non-validated portion.
6. A method according to claim 1 further comprising:
dumping the call stack to isolate the error to the routine that caused the rewrite.
7. A method for allocating memory segments so as to provide for detecting memory corruption comprising:
at initial memory segment allocation, providing a redundant portion at the logical end of a memory segment, said redundant portion containing data derived from an initial header portion of said segment; and
providing a verify memory routine for comparing said redundant portion to said initial portion to determine if an erroneous overwrite has occurred.
8. A method for detecting and correcting memory corruption comprising:
upon accessing a memory segment, comparing a redundant portion at the end of said segment to an initial header portion of said segment;

if said comparing indicates a difference between said segments, determining which portion is valid; and

from said valid portion, reconstructing said invalid portion.

9. A method according to claim 8 wherein said comparing determines if said initial portion and said redundant portion are identical.
10. A method according to claim 8 wherein said determining which portion is valid comprises for each portion comparing stored data in that portion against a check sum value.
11. A method according to claim 8 wherein said determining which portion is valid comprises for each portion determining if a pointer in that portion is within a memory pool range.
12. A buffer system able to detect buffer corruption comprising:
 - a plurality of buffers (110, 120, 130) with logically contiguous addressing;
 - a least one buffer comprising an initial portion (110a) and a final portion (110b);
 - a detector for determining that a write has been performed on said at least one buffer;
 - a comparater for comparing said initial portion and said final portion after a write; and
 - a signaler for sending an alert when said comparater indicates an erroneous overwrite has occurred wherein said signaler can cause stack to be dumped and other debug information to be collected.
13. An information processing system comprising:
 - a process space (500) containing a plurality of executable logic components;
 - buffer allocation logic (510) able to establish a buffer structure in a memory space (550);
 - buffer write logic (520) able to write data to buffers; and
 - buffer verify logic (530) able to determine if an overwrite has occurred by comparing a header portion and an initial portion of a written to buffer.
14. The device according to claim 13 further comprising:
 - repair logic (540) able to repair an overwritten portion.
15. The device according to claim 13 further comprising:

16. An apparatus according to claim 12 wherein said apparatus is embodied into a fixed media containing logic instructions that when loaded into appropriately configured computer systems will cause the system to embody said buffer system.

ABSTRACT OF THE DISCLOSURE

Memory segment overwrites are detected by providing a redundant header at the end of a segment and comparing a redundant header to an initial header. In specific embodiments, overwrites may be detected both after segment writes and prior to buffer reads. In further embodiments, some header overwrite errors may be corrected to increase the mean time between failure of a logic system.

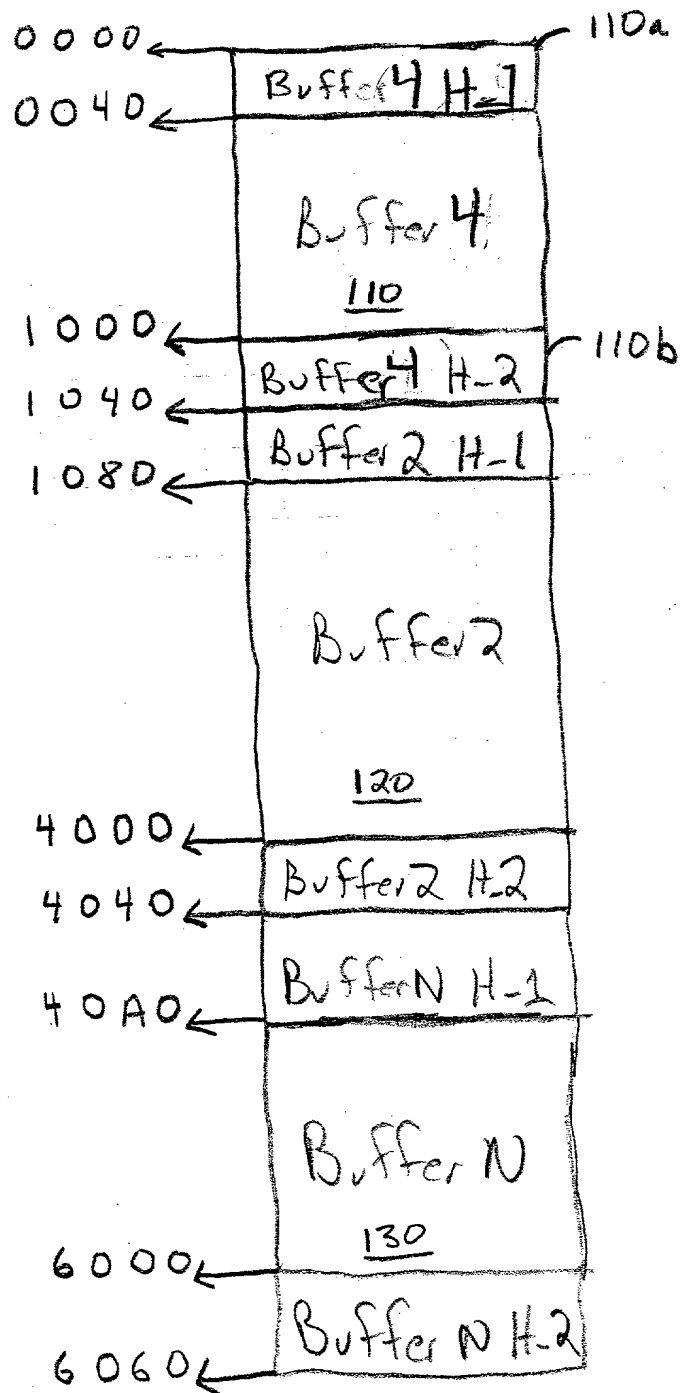


FIG. 1

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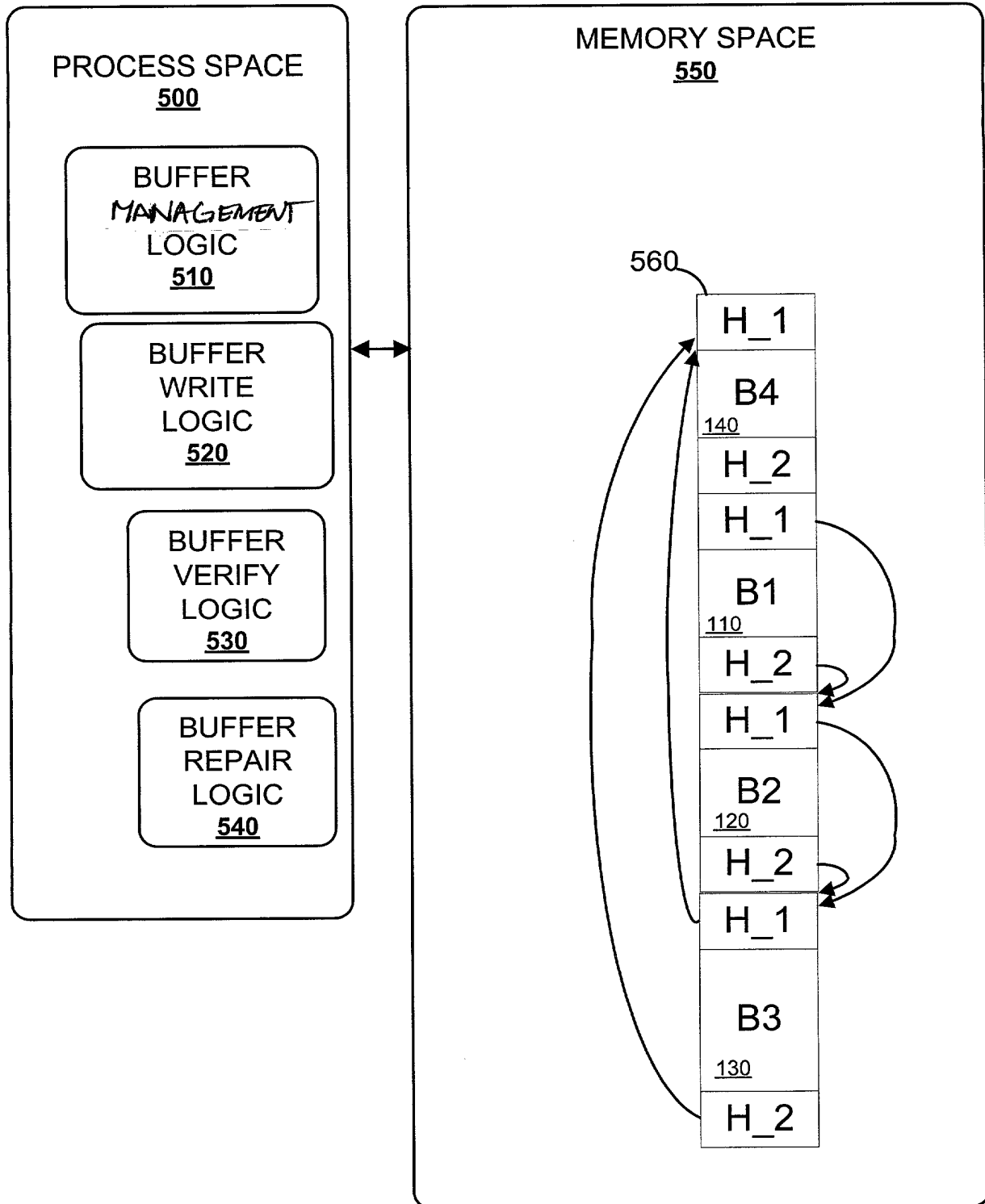


FIG. 5

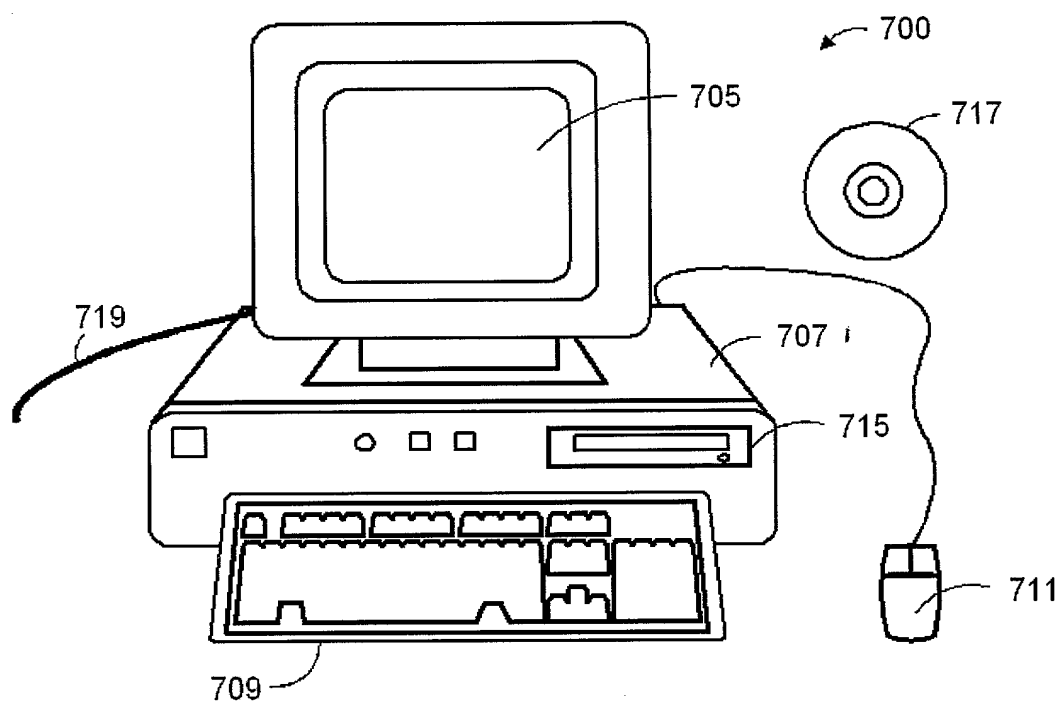


FIG. 6

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

APPARATUS AND METHOD FOR DATA BUFFERING

the specification of which (check one)

X is attached hereto.
 ___ was filed on _____ as Application Serial No. _____
 and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

Priority claimed

(Number)	(Country)	(Day/month/year filed)	Yes	No
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(Number)	(Country)	(Day/month/year filed)	Yes	No
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(Number)	(Country)	(Day/month/year filed)	Yes	No
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I hereby claim the benefits under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose

material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
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(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
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I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application listed below:

(Application Serial No.)	(Filing date)	(Status)
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Power of Attorney: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

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I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the State Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Daniel Wu

Inventor's signature:

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8/1/2000

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